Claims

1. Method for preventing overflow within a digital IIR filter, wherein the filter uses a feedback signal to modify an incoming signal, wherein the feedback signal comprises a sequence of bits, comprising discarding at least one bit from the feedback signal.

2. The method according to claim 1, further comprising increasing the precision with which a feedback signal is recorded.

3. The method according to claim 2, further comprising buffering the feedback signal with double precision.

4. The method according to claim 1, further comprising discarding a least significant bit of the feedback signal.

5. The method according to claim 1, further comprising shifting the feedback signal one bit toward a less significant bit.

6. The method according to claim 1, further comprising communicating the feedback signal to a microprocessor.

7. The method according to claim 1, further comprising receiving the incoming signal.

8. The method according to claim 1, further comprising modifying the incoming signal using the feedback signal to produce a modified signal.

9. The method according to claim 8, further comprising multiplying the modified signal by a scaling coefficient.

10. The method according to claim 8, further comprising outputting the modified signal.

11. The method according to claim 1, further comprising determining when discarding a bit from the feedback signal is required to avoid overflow.

12. An apparatus for preventing overflow within a digital IIR filter, wherein the filter uses a feedback signal to modify an incoming signal, wherein the feedback signal comprises a sequence of bits, comprising:

a memory;

program code configured to initiate the storage of the feedback signal within the memory, wherein program code is further configured to initiate the discarding of at least one bit from the feedback signal.

a microprocessor operable to execute program code.

13. The apparatus of claim 12, wherein the program code initiates the storage of the feedback signal with increased precision,

14. The apparatus of claim 12, wherein program code initiates the discarding of a least significant bit of the feedback signal.

15. The apparatus of claim 12, wherein program code initiates the buffering of the feedback signal with double precision.

16. The apparatus of claim 12, wherein program code initiates communication of the feedback signal to the microprocessor.

17. The apparatus of claim 12, wherein program code initiates reception of the incoming signal.

18. The apparatus of claim 12, wherein program code initiates a shift of the feedback signal one bit toward a least significant bit.

19. The apparatus of claim 12, wherein program code initiates production of a modified signal by using the feedback signal to modify the incoming signal.

20. The apparatus of claim 19, wherein program code initiates multiplication of the modified signal by a scaling coefficient.

21. The apparatus of claim 19, wherein program code initiates outputting the modified signal.

22. The apparatus of claim 12, wherein program code initiates detection of an overflow occurrence prior to discarding a bit from the feedback signal.

23. A program product for preventing overflow in a digital IIR filter, comprising:

a program configured to initiate storage within a memory of a feedback signal, wherein the feedback signal is stored with increased

precision, wherein the program initiates the discarding of at least one bit from the feedback signal, wherein the filter uses the feedback signal to modify an incoming signal, wherein the feedback signal comprises a sequence of bits; and

a signal bearing medium bearing the program.

24. The program product of claim 23, wherein the signal bearing medium includes a recordable medium.

25. The program product of claim 23, wherein the signal bearing medium includes a transmission type medium.